STW9N150

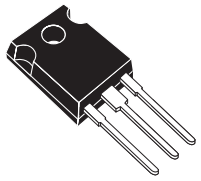
N-channel 1500V - 2.2Ω - 8A - TO-247
Very high voltage PowerMESH™ Power MOSFET

TARGET SPECIFICATION

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STW9N150	1500V	< 2.7Ω	8A	350W

- 100% avalanche tested
- Avalanche ruggedness
- Gate charge minimized
- Very low intrinsic capacitances
- High speed switching
- Very low on-resistance

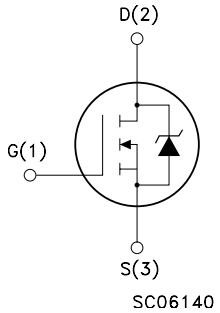


TO-247

Description

Using the well consolidated high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of Power MOSFETs with outstanding performances. The strengthened layout coupled with the Company's proprietary edge termination structure, gives the lowest $R_{DS(on)}$ per area, unrivalled gate charge and switching characteristics.

Internal schematic diagram



Applications

- Switching application

Order code

Part number	Marking	Package	Packaging
STW9N150	W9N150V	TO-247	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	1500	V
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25°C	8	A
I_D	Drain current (continuous) at T_C = 100°C	5	A
I_{DM} (1)	Drain current (pulsed)	32	A
P_{TOT}	Total dissipation at T_C = 25°C	350	W
	Derating factor	0.37	W/°C
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area

Table 2. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	0.36	°C/W
Rthj-amb	Thermal resistance junction-ambient max	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	Tbd	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, I_D = I_{AR}, V_{DD} = 50V)	Tbd	mJ

2 Electrical characteristics

(Tcase =25°C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1mA, V_{GS} = 0	1500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0) V_{DS} = Max rating V_{DS} = Max rating, T_C=125°C				10 500	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 30V			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	3	4	5	V
$R_{DS(on}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 1.3A		2.2	2.7	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 30V, I_D = 2A		Tbd		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0		3600 280 35		pF pF pF
R_g	Gate input resistance	f=1MHz Gate DC Bias=0 Test signal level=20mV open drain		2		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 600V, I_D = 2.5A, V_{GS} = 10V *(see Figure 2)*		90 Tbd Tbd		nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 750V, I_D = 2A, R_G = 4.7Ω, V_{GS} = 10V *(see Figure 1)*		Tbd Tbd Tbd Tbd		ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				8 32	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 4A, V_{GS} = 0			Tbd	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 4A, di/dt = 100A/µs V_{DD}= 45V Tj = 25°C *(see Figure 3)*		Tbd Tbd Tbd		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 4A, di/dt = 100A/µs V_{DD}= 45V Tj = 150°C *(see Figure 3)*		Tbd Tbd Tbd		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300µs, duty cycle 1.5%

3 Test circuits

Figure 1. Switching times test circuit for resistive load

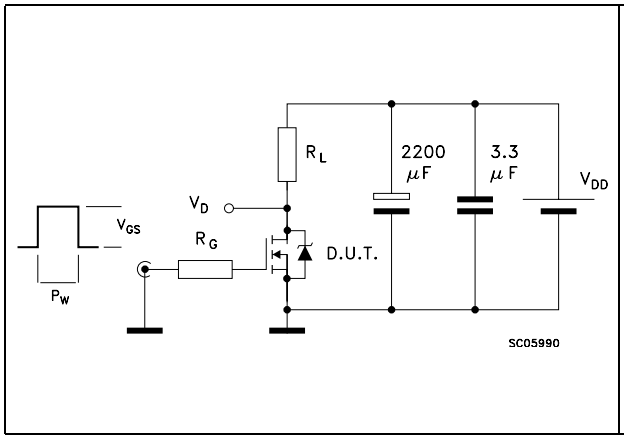


Figure 2. Gate charge test circuit

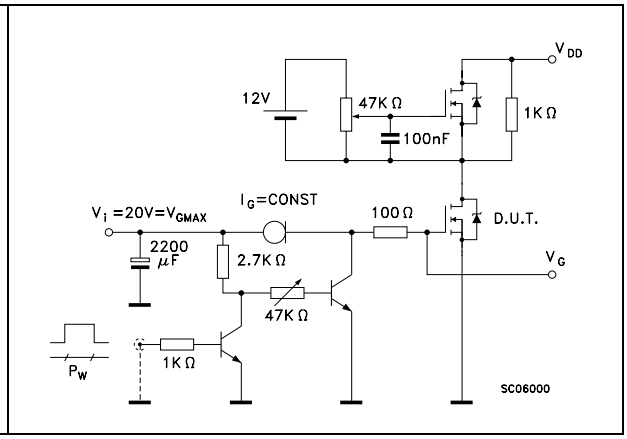


Figure 3. Test circuit for inductive load switching and diode recovery times

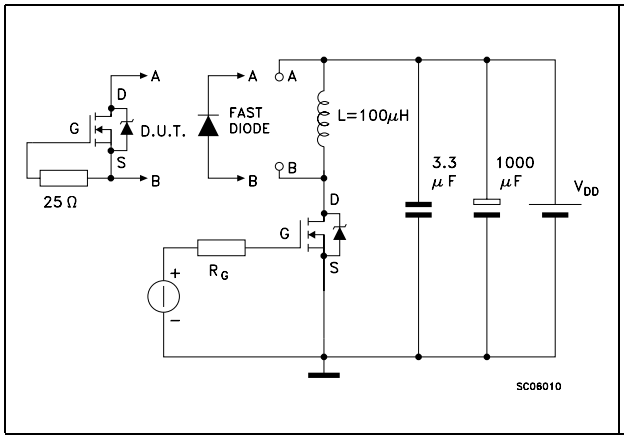


Figure 4. Unclamped Inductive load test circuit

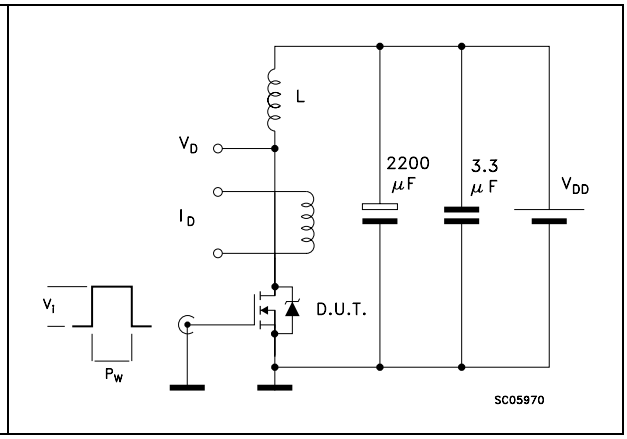


Figure 5. Unclamped inductive waveform

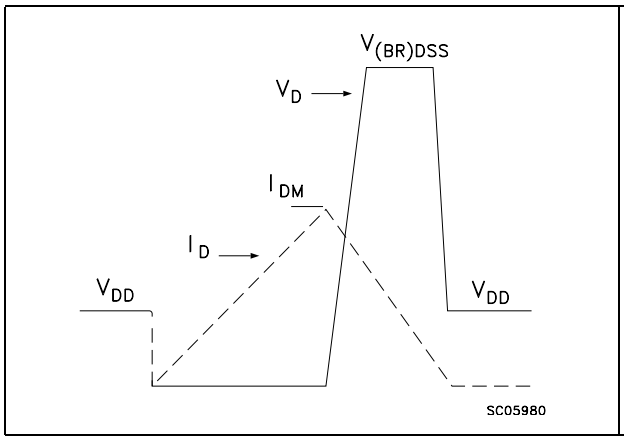
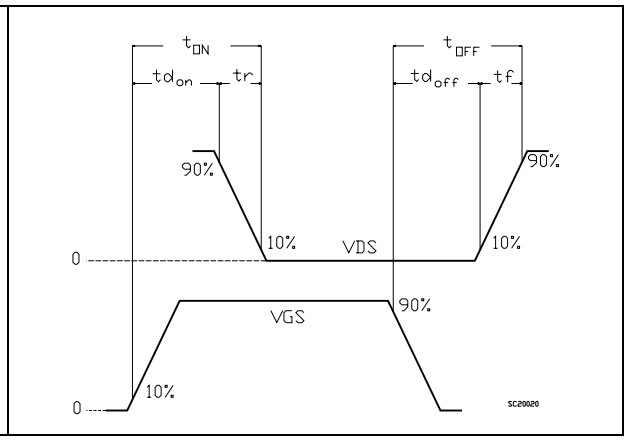


Figure 6. Switching time waveform

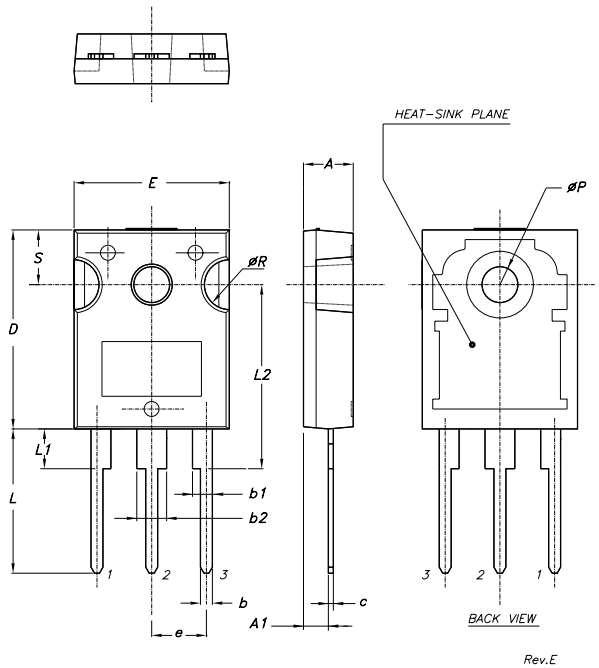


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



5 Revision history

Table 8. Revision history

Date	Revision	Changes
24-May-2007	1	First release

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